CSCI 2330 – Direct-Mapped Caching Exercises

Suppose you have a system with an 8-bit word size and a direct-mapped cache with 8 cache lines and a 4-byte block size. Assume write-back, write-allocate cache behavior.

1. Assuming that every possible address is valid, how many **blocks** of memory exist?

2. How many different memory blocks are mapped to each cache line?

3. When using a memory address to locate data in the cache, how many **index bits**, **offset bits**, and **tag bits** will there be?

4. Suppose that the cache has the contents pictured below.

Consider each of the memory operations listed below, assuming that each operation is either reading or writing a single byte at the given address (which is specified in binary for convenience). For each operation, indicate:

(i) whether the operation results in a **cache hit** or **cache miss**,
(ii) **how many memory blocks are read or written** by the operation (i.e., how many trips to memory itself are required), and
(iii) the **affected cache line with any updates** resulting from the operation.

For writes, the specified value is the byte value that is being written to memory. For reads, the specified value is the byte value that is ultimately returned by the operation (which might be retrieved either from the cache or from memory).

(a) Read 01000100 (byte value 5)

(b) Read 11100000 (byte value 17)

(c) Write 01110000 (byte value 7)

(d) Read 10101000 (byte value 12)

(e) Read 01101100 (byte value 2)

(f) Write 11111100 (byte value 3)

Line	V	D	Tag	Data (4 Bytes)
0	1	0	111	17
1	1	0	011	9
2	0	0	101	15
3	1	1	001	8
4	1	0	011	4
5	0	0	111	6
6	0	0	101	32
7	1	0	110	3