CSCI 2330 – Associative Caching Exercises

1. Consider an associative cache of effective size **C** bytes (i.e., the number of data bytes the cache can hold), where **S** is the number of sets, **E** is the number of lines per set, and **B** is the block size in bytes. Write an expression for E in terms of S, B, and C.

2. On a system with an 8-bit word size, consider a cache with (S, E, B) = (8, 2, 4) and the partial contents shown below. In this cache, a single LRU bit in each set indicates which line in the set was least recently used: if the LRU bit is 0, then the 1st line is LRU, while if the LRU bit is 1, then the 2nd line is LRU. For each of the following memory operations, indicate whether a cache hit or cache miss occurs and note any updates to the affected cache set/line (e.g., LRU bit changes to 1, data value changes to N, etc.). Consider each operation from the **same starting contents** shown below.

   a. Read 11100100 (Value: 9)

   b. Read 11100000 (Value: 17)

   c. Read 01100100 (Value: 7)

   d. Write 01000100 (Value: 10)

   e. Write 01100000 (Value: 2)

Set #	LRU	V	D	Tag	Data (4 Bytes)	V	D	Tag	Data (4 Bytes)
0	1	0	0	111	4	1	0	001	17
1	0	1	1	111	9	1	0	010	5
2				…	…			…	…
3									
4									
5									
6									
7									

3. Decide which word correctly completes the following statement (and why):

"In any cache that has at least 2 cache sets (i.e. a non-fully-associative cache), two adjacent memory blocks (e.g., the two 4-byte blocks consisting of addresses [0-3] and [4-7], respectively) are **[always / sometimes / never]** *mapped to the same cache set."*

Sketching an example will be helpful (e.g., write out addresses in terms of tag/set/offset bits for two adjacent blocks).