# CSCI 2330 – Caching Exercises

1. Consider a cache described by (S, E, B) as detailed in class – S is the number of sets, E is the number of lines per set, and B is the block size. Also let C be the total size of the cache. Give an expression for E in terms of S, B, and/or C, assuming the cache is **fully associative**.

2. Suppose you have written a program to run on a system containing only L1 cache and main memory. Assume that accessing L1 cache takes 1 cycle, while accessing memory takes an additional 100 cycles. Your program presently exhibits a 97% cache hit rate.

You restructure your program's loops to improve its locality, and find that the cache hit rate increases to 99%. Your friend tells you that this clearly was a waste of your time for such a minor improvement. Do you agree? Demonstrate by calculating the average access time before and after.

3. Consider a cache with (S, E, B) = (8, 2, 4), 8-bit memory addresses, and the partial contents shown below. Note that the LRU bit means either the 1st line in the set was least recently used (LRU = 0) or the 2nd line in the set was least recently used (LRU = 1). Sketch the changes that will occur for each of the following memory operations.

a. Read 01000100 (Value: 5)
b. Read 11100010 (Value: 17)
c. Write 01100100 (Value: 7)
d. Read 01000110 (Value: 5)
e. Write 01100000 (Value: 2)

| Set # | LRU | V | D | Tag | Data (4 Bytes) | V | D | Tag | Data (4 Bytes) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 111 | 4 | 1 | 0 | 001 | 17 |
| 1 | 0 | 1 | 1 | 111 | 9 | 1 | 0 | 010 | 5 |
| 2 | | | | … | … | | | … | … |
| 3 | | | | | | | | | |
| 4 | | | | | | | | | |
| 5 | | | | | | | | | |
| 6 | | | | | | | | | |
| 7 | | | | | | | | | |