

Arithmetic Operations

<code>addq</code>	<code>Src, Dest</code>	<code>Dest = Dest + Src</code>	
<code>subq</code>	<code>Src, Dest</code>	<code>Dest = Dest - Src</code>	
<code>imulq</code>	<code>Src, Dest</code>	<code>Dest = Dest * Src</code>	
<code>sarq</code>	<code>Src, Dest</code>	<code>Dest = Dest >> Src</code>	Arithmetic Logical Also called <i>shlq</i>
<code>shrq</code>	<code>Src, Dest</code>	<code>Dest = Dest >> Src</code>	
<code>salq</code>	<code>Src, Dest</code>	<code>Dest = Dest << Src</code>	
<code>xorq</code>	<code>Src, Dest</code>	<code>Dest = Dest ^ Src</code>	
<code>andq</code>	<code>Src, Dest</code>	<code>Dest = Dest & Src</code>	
<code>orq</code>	<code>Src, Dest</code>	<code>Dest = Dest Src</code>	
<code>incq</code>	<code>Dest</code>	<code>Dest = Dest + 1</code>	
<code>decq</code>	<code>Dest</code>	<code>Dest = Dest - 1</code>	
<code>negq</code>	<code>Dest</code>	<code>Dest = -Dest</code>	
<code>notq</code>	<code>Dest</code>	<code>Dest = ~Dest</code>	
<code>leaq</code>	<code>Src, Dest</code>	<code>Dest = Src (as expr)</code>	No memory access!

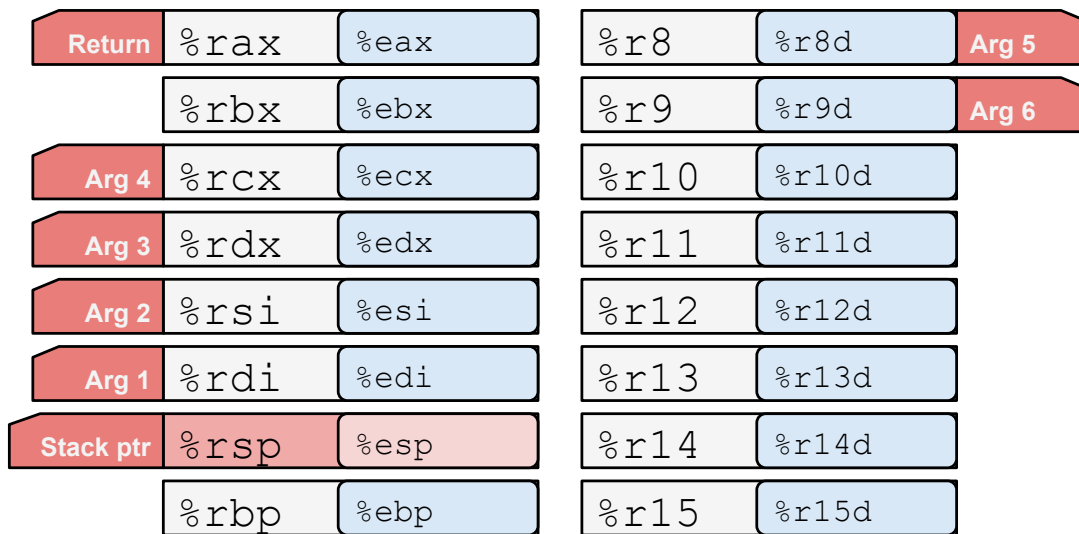
Arithmetic Example

```
long arith
(long x, long y, long z)
{
    long t1 = x+y;
    long t2 = z+t1;
    long t3 = x+4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}
```

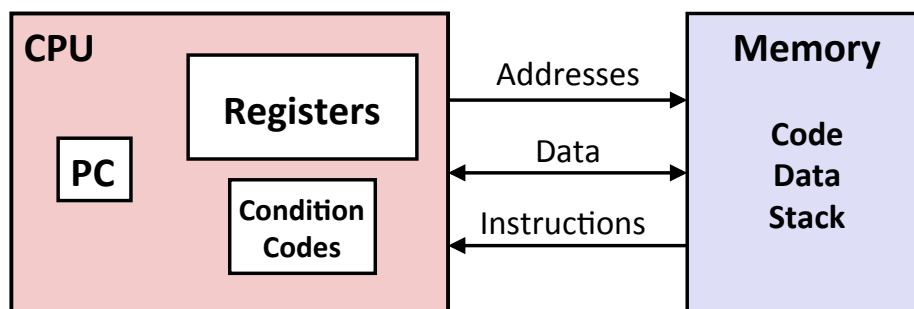
$(x, y, z) \rightarrow (\%rdi, \%rsi, \%rdx)$

```
arith:
    leaq    (%rdi,%rsi), %rax
    addq    %rdx, %rax
    leaq    (%rsi,%rsi,2), %rdx
    salq    $4, %rdx
    leaq    4(%rdi,%rdx), %rcx
    imulq   %rcx, %rax
    ret
```

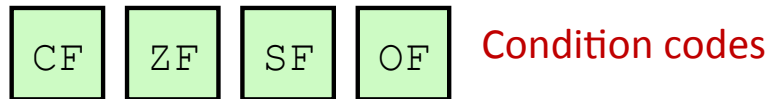
Procedure Call Registers



Assembly View of the Machine



Condition Codes



CF: Carry flag (for unsigned)

ZF: Zero flag

SF: Sign flag (for signed)

OF: Overflow flag (for signed)

Reading Condition Codes

SetX	Condition	Description
sete	ZF	Equal / Zero
setne	\sim ZF	Not Equal / Not Zero
sets	SF	Negative
setns	\sim SF	Nonnegative
setg	\sim (SF^OF) & \sim ZF	Greater (Signed)
setge	\sim (SF^OF)	Greater or Equal (Signed)
setl	(SF^OF)	Less (Signed)
setle	(SF^OF) ZF	Less or Equal (Signed)
seta	\sim CF & \sim ZF	Above (unsigned)
setb	CF	Below (unsigned)

Recap: Single-Byte Virtual Registers

%rax	%al	%r8	%r8b
%rbx	%bl	%r9	%r9b
%rcx	%cl	%r10	%r10b
%rdx	%dl	%r11	%r11b
%rsi	%sil	%r12	%r12b
%rdi	%dil	%r13	%r13b
%rsp	%spl	%r14	%r14b
%rbp	%bpl	%r15	%r15b

Example: Greater Than

```
int gt (long x, long y)
{
    return x > y;
}
```

Register	Use(s)
%rdi	Argument x
%rsi	Argument y
%rax	Return value

```
cmpq    %rsi, %rdi    # Compare x:y
setg    %al           # Set when >
movzbl  %al, %eax     # Zero rest of %rax
ret
```